ANALOG IMPLEMENTATION OF EROSION/DILATION, MEDIAN and ORDER STATISTICS FILTERS

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ABSTRACT

In this work an analog implementation of non-linear filters based on a current-mode sorting/selection network is presented. Three non-linear filters, an erosion/dilation, a median and an order statistics filter are implemented. The circuits are designed using a new high-speed and very accurate current maximum and minimum selector. These filters could be easily incorporated to smart sensors as well as to smart cameras. SPICE simulation results demonstrate the feasibility of simple analog filters using current-mode techniques.

I. INTRODUCTION

Nonlinear order statistics filters is a well known filter class based on data ordering within the filter window [1,2]. They behave very well in impulsive noise removal, where linear filters fail. When properly designed in the form of L-filters, they can cope with different noise probability distributions [1]. It can be easily proven that the basic mathematical morphology operators erosion/dilation of a function by set are essentially a special case of order statistics filters. Furthermore, they can be used as local signal dispersion estimators. As a result, this filters class has been extensively used both in signal and image processing.

Let x_i $i=1,...,N$ be a sampled (digital or analog) signal. Let us use a filter window of odd size $n=2v+1$. The data samples x_{i+j} , $j=-v...v$ within the filter window form the filter output. If we order them, we obtain the ordered samples $x_{(1)} \leq x_{(2)} \leq ... \leq x_{(n)}$ which are also called order statistics [3]. $x_{(1)}$ is the minimum sample and $x_{(n)}$ is the maximum sample within the filter window. The output $x_{(v+1)}$ is the local signal median. The local max/min operators correspond to the erosion/dilation of the signal x_i by set equal to the filter window.

Sorting (ordering) and max/min selection are classical topics in computer science [4]. Several topologies have been proposed for data sorting, called sorting networks. Such a network used for sorting $n=5$ signal samples is shown in Fig. 1. It is called odd/even transportation network. The vertical bars denote max-min selectors of the form:

$$y_1=max\{x_1,x_2\} \tag{1}$$

$$y_2=min\{x_1,x_2\} \tag{2}$$

which form the basic building block of the network. A variety of such sorting or order selection network can be formed in [1,4]. A special case for median calculation of $n=9$ signal samples is shown in Fig. 2. Again max/min selector is the basic building block. Finally a max/min (erosion/dilation) network is shown in Fig. 3.

In the following, we shall concentrate our efforts in proposing filter architectures that are suitable to order statistics filtering and that are easily implemented in a hybrid (analog/digital) way. The motivation to built these architectures is to construct fast, simple and affordable filters that operate directly on the analog signal and can be easily incorporated to smart sensors as well as into smart cameras. However, there are only few publications on analog realization [5-9] and three recent current-mode designs [10,12]. The proposed architectures are essentially suited to one dimensional signal filtering (e.g sound, ECG/EEGS, measurements). However, similar architectures and their implementation can be used for two-dimensional signal (image) processing.

II. THE CURRENT-MODE MIN/MAX SELECTOR CIRCUIT

A. The block diagram of the min/max current selector

In nonlinear filtering based on order statistics, a basic operation is to compare signal samples and change their position according to their relative rankings. This section explains the operation of a new current-mode min-max selector which sorts its input currents in ascending order by determining I_{max}=max{ I_1,I_2} and I_{min}=min{ I_1,I_2} at its outputs.

Fig.4 shows the block diagram of the proposed min/max current selector. The input stage consists of two delay elements feeding the two PMOS input current mirrors with currents I_1 and I_2. These currents are mirrored into the basic current maximum circuit [13] as well as to the swap circuit. The feedback circuit is used to correct the corner error of the current maximum circuit. Two high speed current comparators *comp1* and *comp2* are driven by the current maximum circuit. V_{o1} and V_{o2} are their digital outputs that change the position of currents I_1 and I_2 at the swap circuit according to their relative rankings.

B. The delay elements

Since filtering of serial input data involves sampling the input periodically, a clock delay circuit is needed to sample the signal and to synchronize the data flow in the structure. In this work, a delay line has been used based on the well-known switched-current (SI) technique, described in detail in [12,14].

C. The current maximum circuit

The two input current mode maximum circuit is shown in Fig.5. Each maximum cell for an input current is formed by the transistor pairs M_{11}-M_{12}, and M_{21}-M_{22}. The current I_b of the diode connected transistor M_b is used as the current source of the circuit. Furthermore this circuit is modified to have two outputs instead of one as stated in [13].

The equilibrium state implies that only one of the output paths M_{12},M_{22} is in conduction, the drain current of M_b is the exact replica of the maximum input current. We suppose that I_1>I_2. The drain

voltages V_{D1} and V_{D2} of the transistors M_{11} and M_{21} respectively, are established by the input currents I_1 and I_2 and $V_{D1} > V_{D2}$ since the voltage V_{D1} is established by the maximum input current. The transistors M_{11},M_{21} are regarded as a differential transistor pair.

At the steady state, when the voltage difference V_{dif} between V_{D1} and V_{D2} satisfies the equation

$$V_{dif} = \left|V_{D1} - V_{D2}\right| \geq \sqrt{2I_b / \beta} \tag{3}$$

(where $\beta=\mu C_{ox}/2)\, W/L$, μ is the electron mobility, C_{ox} is the gate oxide capacitance of the MOS, W is the channel width and L is the channel length of the MOS), the currents will flow through the transistor of the differential pair with the maximum input voltage. Thus, the output current I_{o1} will be equal to I_b and the current I_{o2} will be zero. Transistors M_b and M_{11} then form a current mirror and the current I_b is equal to the maximum input current I_1. According to the above considerations the output currents are $I_{o1}=I_1$ and $I_{o2}=0$. Only one output current of the current maximum circuit is equal to the maximum input current (and different to zero), while the other output is zero.

The inherent problem associated with this implementation is the «corner error" in the transition region of the current maximum circuit. When eq.(3) is not satisfied, the two output currents do not have the correct values.

D. High speed current comparator

Fig. 6 shows a high-accuracy and high-speed current comparator [15]. This comparator can operate for low voltage supplies and the operation speed is not limited due to the overlapping capacitor of the MOS transistor (Miller effect). Furthermore, the operation is virtually insensitive to technological-parameters. The circuit employs nonlinear negative feedback to obtain high-accuracy, less than 1.5pA, and high-speed operation down to 10ns.

E. The overall structure of the min/max selector with the corner error correction

The complete min/max selector circuit is shown in Fig. 7. The currents I_1 and I_2 are its inputs and the currents I_{max} and I_{min} are its outputs. The currents I_{o1} and I_{o2} are mirrored into the feedback circuit via the PMOS current mirrors M_{i3}-M_{i4}-M_{i5} (i=1,2) as well as into the subtraction nodes A_1 and A_2. The transistors M_{C1} and M_{C2} are identical so their drain currents are equal to:

$$I_f = \frac{I_{o1} + I_{o2}}{2} \tag{4}$$

The feedback current I_f is mirrored to the subtraction nodes A_1 and A_2 via the current mirror M_{C1},M_{16} and M_{26}. As a result, the currents at the input of the current comparators I_{C1}, I_{C2} are the difference between each output current and the feedback current I_f and are given by:

$$I_{Ci}=I_{oi}-I_f \quad \text{for i=1,2} \tag{5}$$

At the beginning, we assume that at steady state $I_1>I_2$, as shown in Fig. 8a. Thus, the feedback current I_f is equal to $I_f = \frac{I_1}{2}$. Using eqns(4,5), we extract the following:

$$I_{Ci} = \begin{cases} I_1 - \frac{I_1}{2} = \frac{I_1}{2} & i=1 \\ 0 - \frac{I_1}{2} = -\frac{I_1}{2} & i=2 \end{cases} \tag{6}$$

for the input currents of the comparators.

Thus, current I_{C1} of comp1 which corresponds to the maximum input current is positive, while I_{C2} of current comp2 is negative. Consequently, the digital voltage outputs of the comparators will be :

$$V_{oi} = \begin{cases} \text{'logic one'} \ , & i=1 \\ \text{'logic zero'} \ , & i=2 \end{cases} \tag{7}$$

as shown in Fig. 8b. This means that only the digital output V_{oi} corresponding to the maximum input current (I_1 in our case) is at logic one, while the other one goes to logic zero.

At the transition region where the two inputs are very close to each other, eq(3) is not satisfied. The corner error is associated with the linear operation of M_{11},M_{21} within the transition region as shown in Fig 8a. At the crossing point, where the input currents are equal I_1=I_2, the transistors M_{11},M_{21} have the same drain-source voltage V_{D1}=V_{D2} because their gate-source voltages are always the same. Consequently, M_{12} and M_{22}, which are saturated, produce the same drain currents I_{o1}=I_{o2}=I_o. Thus, the input currents are crossed at the same point with the output currents. At this crossing point, I_f is also equal to I_o since I_f=(I_{o1}+I_{o2})/2=I_f=(I_o+I_o)/2=I_o (Fig. 8a).

Due to feedback circuit every time the two output currents I_{o1} and I_{o2} , which correspond to the old maximum and the new maximum input current, are compared with the feedback current I_f. The output of the circuit during the transition region is:

$$V_{oi} = \begin{cases} \text{'one'} & \text{for } I_{o1} > I_f > I_{o2} \\ \text{'zero'} & \text{for } I_{o1} < I_f < I_{o2} \end{cases} \tag{8}$$

It is clear from eq.(8) that the output V_{o1} is at logic 'one' within the transition region for the case I_1>I_2 (Fig.8b). Using the same considerations for the case that I_2>I_1, the output voltages are flipped, so output V_{o2} is at logic 'one', corresponding to the new maximum input current, while I_1 is at logic 'zero'.

F. Swap circuit

The current swapping circuit employs NMOS differential switches to achieve fast settling time. The swapping operation is realized when the gates of M_{S2} and M_{S3} are driven to logic 'one' via comparator comp2 and at the same time the gates of M_{S1} and M_{S4} are driven to logic 'zero' via comp1. In the opposite case, no swapping operation will be performed.

III. EFFECT OF COMPONENT MISMATCHES

In the preceding analysis, the basic filters operation has been described by neglecting effects such as component mismatches. Mismatches on the transistors aspect ratio, on the oxide thickness and on mobility give rise to mismatch in the transconductance parameters β and on the threshold voltage V_T of the MOS transistors. These mismatches affect the total accuracy of the proposed implementation in two ways. First, they limit the resolution of the min-max selector circuit. Second, affect the accuracy of the current mirrors which are used at every min-max selector circuit in order to convey the input current at the final filter output.

It is assumed that the mismatches between the transistors in β and in V_T are $\Delta\beta$ and ΔV_T respectively. By expanding the well known equation of the MOS transistors which operate in the linear and in the saturation region around the nominal bias point, the drain current mismatch $\Delta I_D/I_D$, in the linear region is given by [16]:

$$\frac{\Delta I_D}{I_D} = \frac{-\Delta V_T}{V_{GS}-V_T} + \frac{\Delta V_{GS}}{V_{GS}-V_T} + \frac{\Delta\beta}{\beta} + \frac{\Delta V_{DS}}{V_{DS}} \tag{9}$$

and in the saturation region by:

$$\frac{\Delta I_D}{I_D} = \frac{-2\Delta V_T}{V_{GS}-V_T} + \frac{2\Delta V_{GS}}{V_{GS}-V_T} + \frac{\Delta\beta}{\beta} \tag{10}$$

We use the above equations in order to calculate the effect of mismatches in the min-max selector circuit. It is assumed that, in the transition region, the transistors M_{11},M_{21} and M_{12},M_{22} operate in the linear and in the saturation region, respectively. Then, the output current mismatch $\Delta I_o/I_o$ of the min-max selector circuit (Fig. 5) is given by:

$$\frac{\Delta I_o}{I_o} = \Delta V_T\left(-\frac{2\beta}{g_{mi2}} + \frac{V_{DS}}{g_{mi2}}\frac{\beta^2}{g_{mi1}}\right) + \frac{\Delta\beta}{\beta}\left(1-\frac{V_{DS}}{g_{mi2}}\beta\right) + \frac{V_{DS}}{g_{mi2}}\beta\frac{\Delta I}{I} \tag{11}$$

where $\beta=\beta_{i1}=\beta_{i2}$, $g_{mi1}=\beta(V_{GSi11}-V_T)$, $g_{mi2}=\beta(V_{GSi2}-V_T)$, $I=I_{o1}=I_{o2}$, $V_{DS}=V_{D1}-V_{SS}=V_{D2}-V_{SS}$, $I=I_1=I_2$ and i=1,2. The drain current mismatch of each current mirror $\Delta I_M/I_M$ is given by

$$\frac{\Delta I_D}{I_D} = \frac{-2\Delta V_T}{(V_{GS} - V_T)} + \frac{\Delta\beta}{\beta_M} \tag{12}$$

where β_M is the transconductance parameters and V_{GS} is the gate-source voltage of the transistors, which form the current mirrors. These mismatches on the current mirrors can be minimised by the careful design of the transistors that form the current mirrors of each min-max selector, separately.

IV. SIMULATION RESULTS

In order to verify the performance of the proposed circuits SPICE simulations were performed on the extracted netlist of the their layout using Cadence design tools with AMS 1.2μm CMOS process parameters. The supply voltage was ±2.5V. The dimensions of the transistors of the high-speed comparator were modified appropriately for the AMS technology parameters. The dimensions of the transistors of the min-max selector are: $(W/L)_{Mi1,Mi2,MB}$=12/1.2, $(W/L)_{Mi3,Mi4,Mi5,MB}$=25/5 and $(W/L)_{Mc1,Mc2,Mi6}$=12/5. In order to improve the accuracy, minimize systematic errors and increase the output resistance of the current mirrors, low-voltage high-swing current mirrors have been used [17]. It should be noted that the effect of spikes on circuit performance, due to the switches feedthrough have been minimized with dummy switches that were used for the simulations of the switched-currents delay lines.

Table I shows the precision attained for the worst case as a function of the input current level, measured through Monte Carlo simulations, and using the statistical parameters reported by Pelgrom et al [18]. In case of the min-max selector, one of its input currents is held constant and the second one was swept around this value, measuring the point at which the transition occurred. The error caused by component mismatches is very small, since this circuit has a symmetrical structure due to the feedback circuit, and the error due to the PMOS current mirrors $M_{13,14,15}$, $M_{23,24,25}$ is partially removed by the error due to the NMOS current mirrors $M_{C1,C2}$-$M_{16,17}$. In case of the three filters shown in Fig.1-3, Monte Carlo simulations shows that accuracy is degraded with increasing

number of comparisons. However even in case of the median filter with window size $n=9$ the error is about 1%. The errors were computed using the following equation :

$$error = \frac{|I_{in} - I_{mean}| + I_{sigma}}{range} \times 100 \tag{13}$$

where I_{mean} , I_{sigma} is the mean value and the standard deviation of the current, respectively and range=29μA.

Finally, to ensure an accurate operation of the proposed filters, a special care must be taken during the layout design. The transistors M_{12} and M_{22} (Fig. 5) were designed using common centroid geometry, while current mirror transistors were split and interdigitized in order to minimize technological parameter errors.

The two input min-max selector circuit has a 10ns response and 10nA resolution. Fig. 9 shows the results for erosion/dilation (max/min) filter having window size equal to 8. The sampling period is 100ns. It is clear that the circuit requires 8 sampling periods for the initialization. After 8 periods the output currents I_{max} and I_{min} take the maximum and minimum value, respectively, for each window. The values of local maximum and minimum input currents remain constant for 8 periods. The accuracy of the max/min filter is limited only by the accuracy of current mirrors and is less than 0.6%. The total delay time is measured to be less than 30ns.

Fig. 10 shows the results for a median filter having window size equal to 9. The input signal is a waveform corrupted with impulsive noise. The sampling period is 200ns. It is clear that the 1MHz ripples and impulsive ringings are removed, while the characteristic shape of the waveform is retained. The accuracy of the median filter is about 1%. The measured delay time of the median filter is approximately equal to 2μs. This delay time is mainly contributed due to the fact that the window size is equal to 9.

Fig. 11a shows the input current for the order statistics filter with window size 5. The filter has 4 constant input currents I_1=20μA, I_2=15μA, I_3=10μA, I_4=5μA, and the 5th input I_5 is a triangular

signal with 25μA amplitude and period 20μs. The outputs of the filter are shown in Fig.11b. The accuracy is better than 0.8% and the delay time is less than 40ns.

All the presented filters may also operate with low supply voltage as +-1.5V, in order to minimize power consumption and meet supply voltage requirements of portable devices.

V. CONCLUSION

Three analog implementations of non-linear filters, an erosion/dilation, a median and an order statistics filter, are presented. The circuits are designed using switched-current delay lines and current-mode sorting/selection network. The comparison block is a new two input analog, current-mode, min/max selector circuit, presenting improved speed and higher accuracy than the conventional ones. Since this is the basic building block for the three filter implementations the output error of the filters is about 1% or less, depending on the number of comparisons as demonstrated by Monte Carlo analysis. These filters could be easily incorporated to smart sensors as well as to smart cameras.

REFERENCES

[1] I.Pitas, A.N.Venetsanopoulos, *Nonlinear digital filters: principles and applications*, Prentice Hall, 1993.

[2] E.R. Dougherty, J. Astola, *An introduction to nonlinear image processing*, SPIE Press, 1974.

[3] H. A. David, *Order statistics,* New York: Wiley, 1980.

[4] D.E. Knuth, *The art of computer programming*, Vol.3, Addison-Wesley,1973.

[5] J. S.J. Lin and W.H. Holmes, ‘‘Analog implementation of median filters for real-time signal processing’’ , *IEEE Trans. Circuits Syst.,* Vol. 35, pp.1032-1033, Aug. 1988.

[6] T. Jarske and O. Vainio, ‘‘A review of median filter systems for analog signal processing’’, *Analog Integr. Circuits and Signal Processing,* Vol. 3, pp. 127-135, 1993.

[7] S. Paul and K. Huper, ‘‘Analog Rank Filtering’’, *IEEE Trans. Circuits Syst.-I: Fundam. Theory and Applic.,* Vol. 40, pp. 469-475, July 1993.

[8] K. Urahama and T. Nagao, ‘‘Direct analog rank filtering’’, *IEEE Trans. Circuits Syst.-I: Fundam. Theory and Applic.,* Vol. 42, pp. 385-388, July 1995.

[9] C.K. Tse and K.C. Chun, ‘‘Design of a switched-current median filter’’, *IEEE Trans. Circuits Syst.-II: Analog and Digital Signal Processing,* vol. 42, pp. 356-359, May 1995.

[10] V.V.B. Rao and D.C. Kar, ‘‘A new analog voltage sorter’’, *IEEE Trans. Instrum. Measur.,* Vol.41, pp. 714-716, Oct. 1992.

[11] J.E. Opris and G.T.A. Kovacs, ‘‘Analogue median circuit’’, *Electr. Letters,* Vol. 30, pp. 1369-1370, Aug. 1994.

[12] S. Siskos, S. Vlassis and I. Pitas, ‘‘Analog implementation of min/max filtering’’, *IEEE Trans. Circuits Syst.-II*, Vol. 45, pp. 913-917, July 1998.

[13] C.-Y. Huang and B.-D. Liu, ‘‘Current-mode multiple input maximum circuit for fuzzy logic controllers’’, *Electron. Lett.,* Vol. 30 , pp. 1924-1925, Nov. 1994.

[14] B. Jonsson and S. Eriksson, «New clock-feedthrough compensation scheme for switched-currrent circuits», *Electr. Lett*., Vol. 29, pp. 1446-1447, 1993.

[15] G. Linan-Cembrano, R. Del Rio-Fernandez, R. Dominguez-Castro and A. Rodriguez-Vazquez, ‘‘Robust high-accuracy high speed continuous-time CMOS current comparator’’, *Electron. Lett.,* Vol. 33 , pp. 2082-2084, Dec. 1997.

[16] C. J. Abel, C. Michael, M. Ismail, C. S. Teng and R. Lahri, ‘‘Charactirization of transistor mismatch for statistical CAD submicron CMOS analog circuits’’,*ISCAS’93* Chicago , pp1401-1404, 1993.

[17] P. J. Crawley and G.W. Roberts, ‘’High-swing MOS current mirror with arbitrarily high output resistance’’, *Electron. Lett.,* Vol. 28, pp. 361-363, Feb. 1992.

[18] M.J.M Pelgrom, A.C.J. Duinmaijer and A.P.G. Welbers, ‘‘Matching properties of MOS transistrs’’, *IEEE J. Solid-State Circuits*, Vol. 24, pp.1433-1440, Oct. 1989.

Table caption

Table I Monte Carlo simulated precision for the proposed min-max selector, order statistics, median and erosion/dilation filter

Figures captions

Fig.1 Odd/even transportation network for n=5. The vertical bars denote max/min selectors.

Fig.2 Median filter structure for n=9.

Fig.3 Erosion/dilation filter structure for n=8.

Fig.4 Block diagram of the min-max selector.

Fig.5 Current maximum circuit.

Fig.6 High speed current comparator and its symbol.

Fig.7 Overall structure of the min-max selector circuit.

Fig.8 Input and output currents (8a), digital outputs (8b).

Fig.9 Input and output of the erosion/dilation filter with window size equal to 8.

Fig.10 Input (10a) and output (10b) of the median filter for *n=9.*

Fig.11 Input currents (11a) and output currents (11b) of the order statistics filter for *n=5.*

Table I

Input Current	Error %			
	Min-Max Selector	Erosion/Dilation	Median	Order Statistics
1uA	0.043	0.38	1.17	0.5
5uA	0.044	0.39	1.18	0.52
10uA	0.029	0.26	0.8	0.35
15uA	0.022	0.23	0.73	0.32
20uA	0.025	0.32	1	0.43
25uA	0.032	0.43	1.1	0.58
30uA	0.039	0.56	1.12	0.75

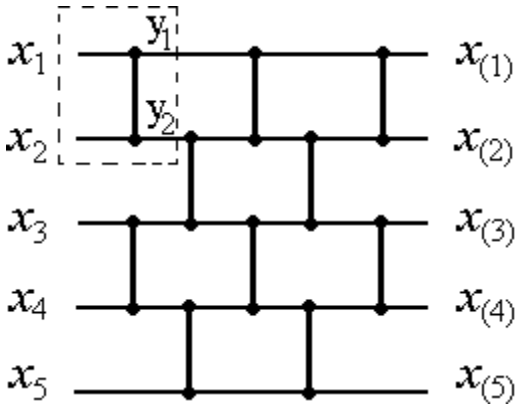


Fig. 1 Odd/even transportation network for n=5. The vertical bars denote max/min selectors

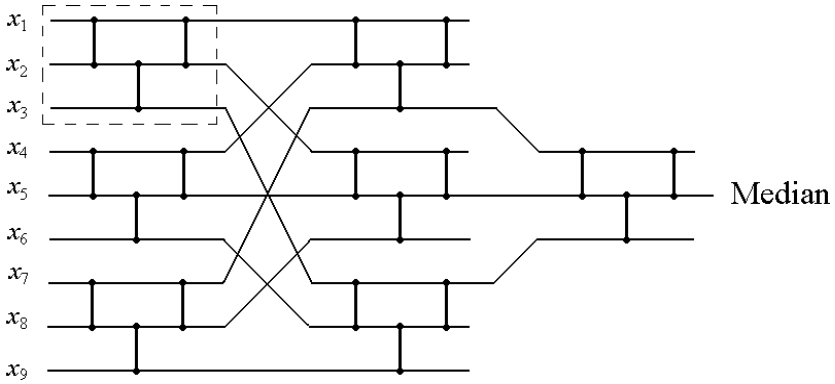


Fig.2 Median filter structure for n=9. The vertical bars denote max/min selectors

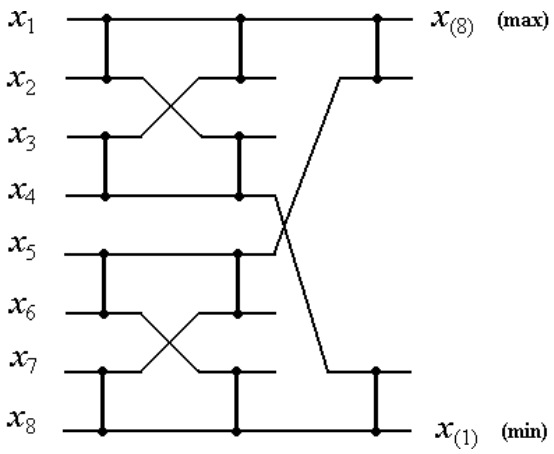


Fig.3 Erosion/dilation filter structure for n=8. The vertical bars denote max/min selectors

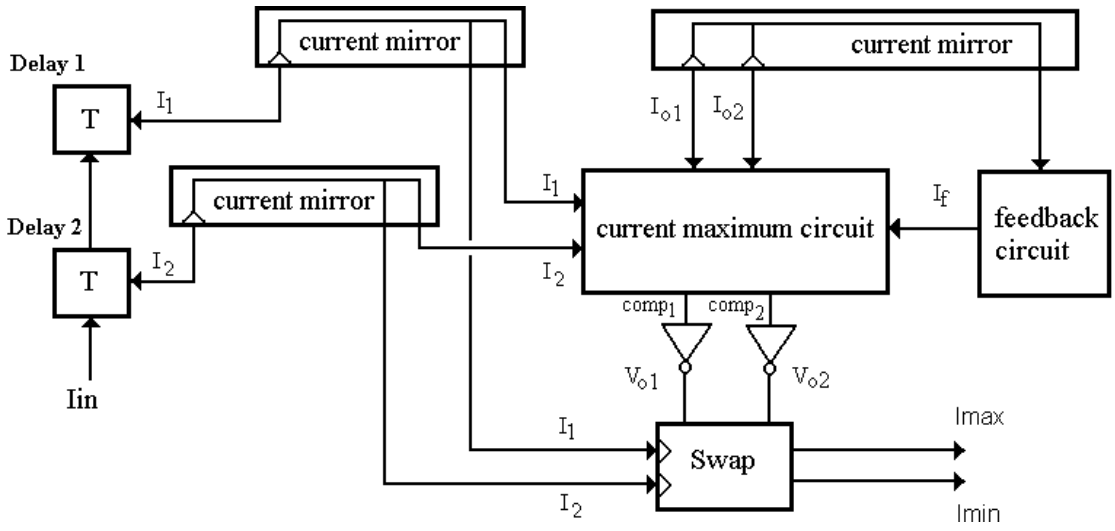


Fig.4 The block diagram of the min-max selector

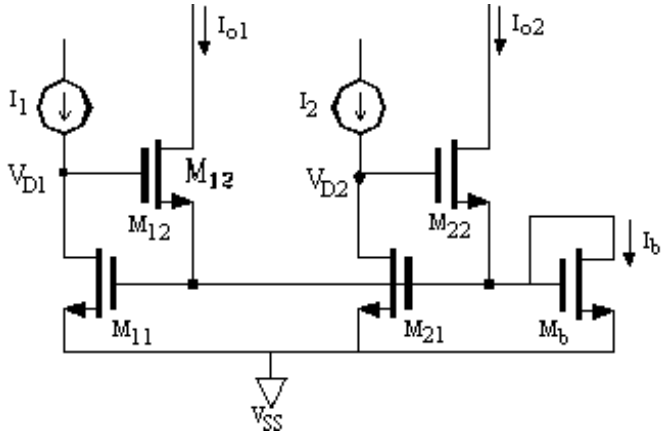


Fig.5 The current maximum circuit

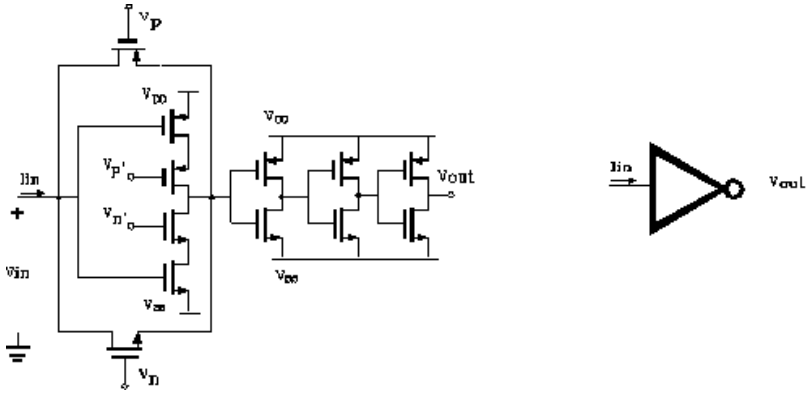


Fig.6 The high speed current comparator and its symbol

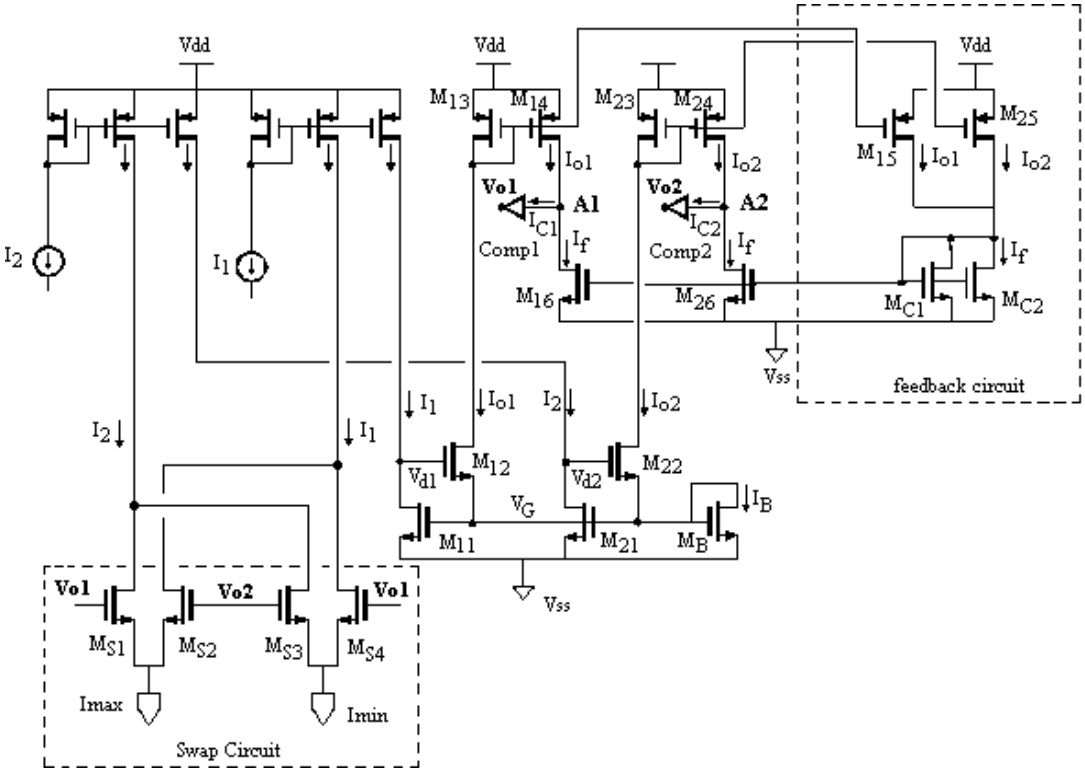


Fig.7 The overall structure of the min-max selector circuit

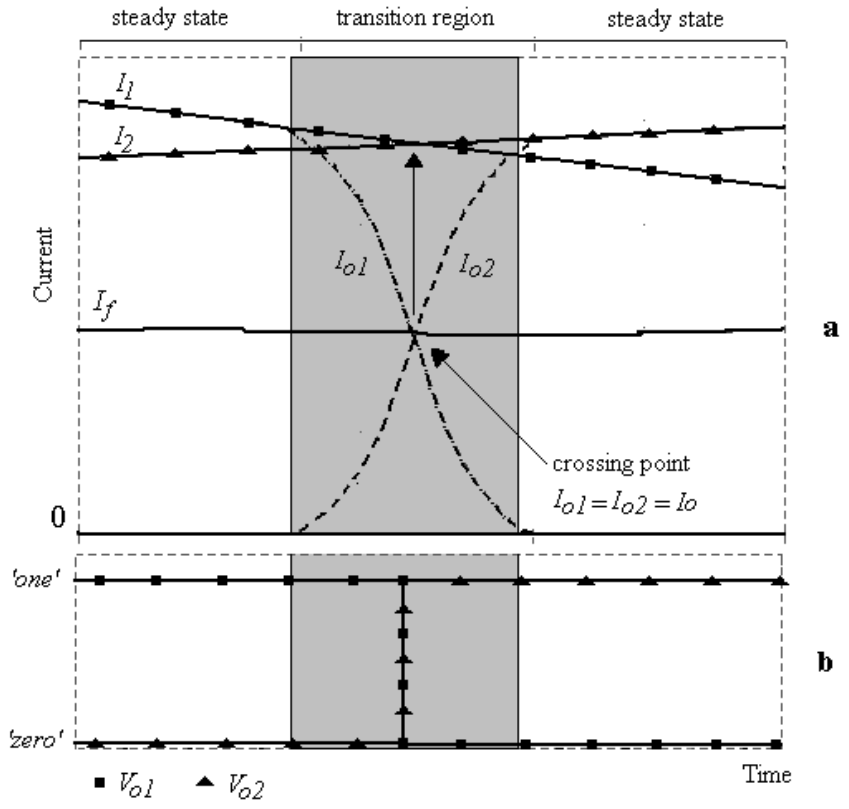


Fig.8 Inputs and outputs current (8a), digital outputs (8b)

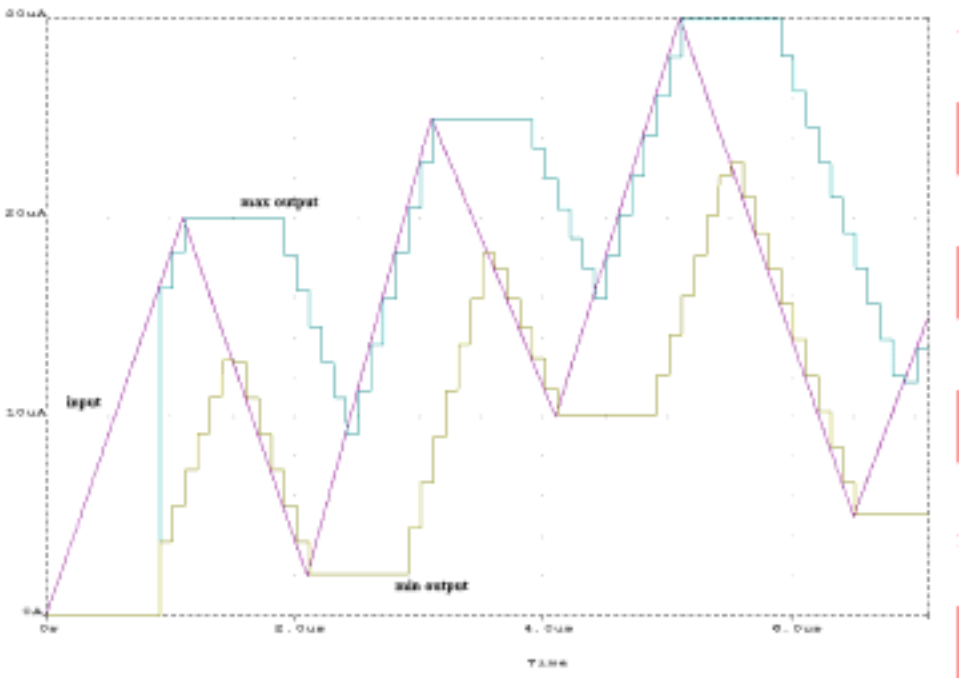
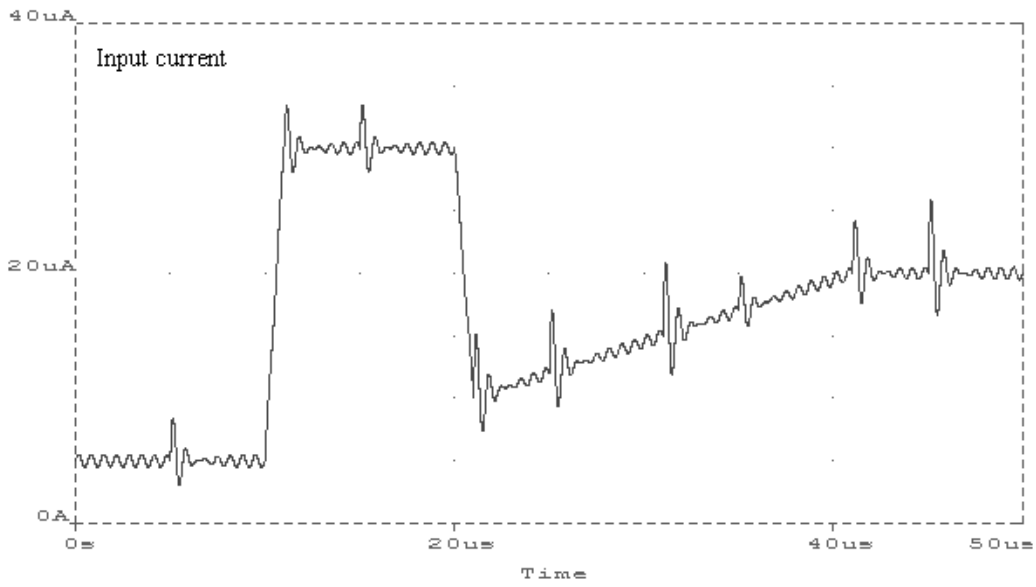
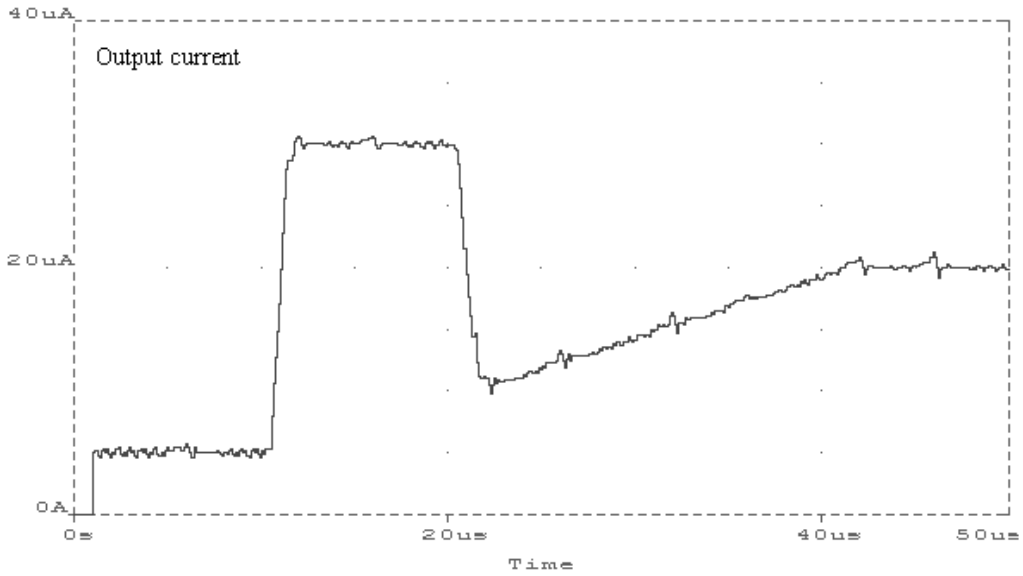


Fig.9 Input and output of the erosion/dilation filter for n=8

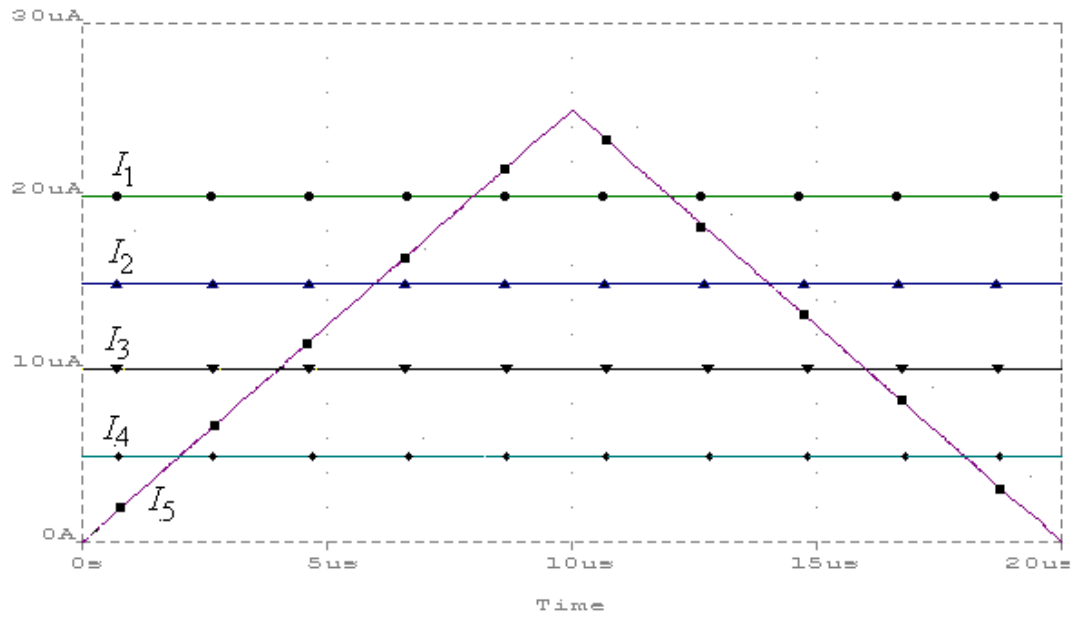


10a

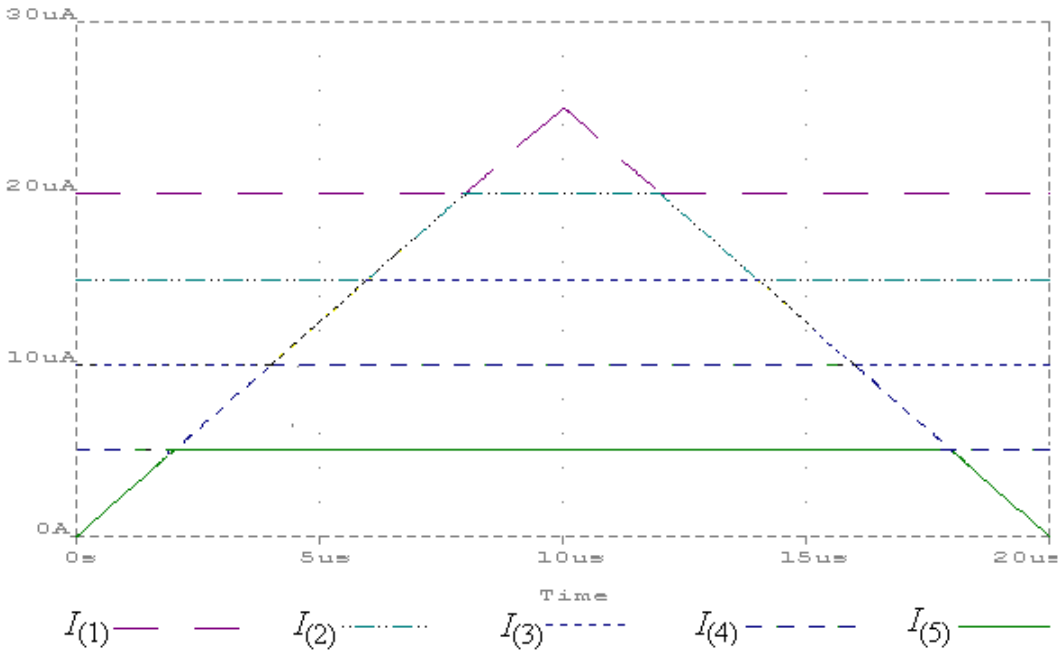


10b

Fig.10 Input (10a) and output (10b) of the median filter for n=9



11a



11b

Fig.11 Input currents (11a) and outputs currents (11b) of the order statistics filter for n=5